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EXAMINER	
LANDAU, MATTHEW C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/611,892	RHODES, HOWARD E.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34,37-46,48-52 and 85-93* is/are pending in the application.

4a) Of the above claim(s) *11,12,23,30,33,44 and 90-93* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-22,24-29,31,32,34,37-43,45,46,48-52 and 85-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Note that claim 33 as amended does not read on the elected species. According to the specification (paragraph [0052]), the reset transistor has an increased gate length only in the three-transistor embodiment (which corresponds to Species IB). Therefore, claims 11, 12, 23, 33, 30, 44, and 90-93 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention/species, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-10, 13, 14, 21, 22, 24-29, 31, 38, 39, 41-43, 45, 50, 51, 85, 86, 88, and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al. (US Pat. 6,166,405, hereinafter Kuriyama) in view of Komuro (US Pat. 5,780,902).

Regarding claims 1 and 2, Figure 5 of Kuriyama discloses a photoconversion device 33; and a first transistor (reset transfer transistor) (col. 11, lines 18-21) having a gate with a first side (left side) and a second side (right side) opposite said first side opposite said first side, said gate being associated with said photoconversion device at said first side of said gate, said first transistor also having a single active area extension region 34b associated with said second side of said gate. The difference between Kuriyama and the claimed invention is a halo implant below

said single active area extension region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous.

Regarding claims 1, 3, 4, 6, and 7, Figure 1 of Kuriyama discloses a photoconversion device 13 (photodiode) (col. 5, line 66 – col. 6, line 5); and a first transistor (charge transfer transistor) (col. 5, lines 20-24) having a gate with a first side (left side) and a second side (right side) opposite said first side, said gate being associated with said photoconversion device at the first side of said gate, said first transistor also having a single active area extension region 14b associated with said second side of said gate. The difference between Kuriyama and the claimed invention is said first transistor has a halo implant region (threshold voltage adjustment implant) in the channel region and extending partially below a gate of said first transistor. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed in the channel (below an LDD region) and partially under the gate electrode. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous. Furthermore, it is known that a halo (pocket)

implant region affects the threshold voltage of a transistor. Therefore, it can be considered that the halo implant is also a threshold voltage adjustment implant. Note that it is considered that the "channel region" is the region between the source and drain.

Regarding claim 8, Figure 1 of Kuriyama discloses said single active area extension region 14b is spaced away from a gate 12 of said first transistor by a portion 11 of a substrate 10/11 supporting said first transistor. Note that insulating film 11 can be considered to be part of the substrate. Therefore, both the active area extension region and the halo implant will be spaced from the gate by a portion of the substrate.

Regarding claim 9, Figure 1 of Kuriyama discloses said photoconversion device 13 is part of a four transistor pixel circuit comprising a transfer transistor as said first transistor (col. 5, lines 20-24), a reset transistor, a source follower transistor (amplification FET), and a row select transistor (select FET).

Regarding claim 10, Kuriyama does not explicitly disclose that at least one of said reset transistor and said source follower transistor (amplification FET) have a single active area extension region. However, as stated above, Figure 1 of Kuriyama discloses a single active area extension region 14b for the transfer transistor. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including an active area extension region (LDD region) in at least one of the reset FET and the amplification FET for the purpose of inhibiting short channel effects and hot carrier generation in those transistors as well as the transfer transistor. Employing an LDD region for the above stated purpose is extremely well known in the art.

Regarding claim 13, the difference between Kuriyama and the claimed invention is said active area extension region said first transistor has a dopant concentration of about 1 x 10^{12} to about 3 x 10^{13} ions/cm^3. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Kuriyama by using the claimed range of dopant concentration, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, Figure 3 of Kuriyama discloses said first transistor has a single insulating spacer, said spacer positioned on said second side (right side) of said transistor.

Regarding claims 21, 22, and 25, Figure 5 of Kuriyama discloses a semiconductor substrate 30, a reset transistor (col. 11, lines 19-21) over said substrate; a photosensor 33 in electrical communication with said reset transistor, said photosensor being within said substrate on a first side of said reset transistor; and a single active area extension region (lightly-doped drain (LDD)) 34b in said substrate adjacent to said reset transistor, said single active area extension region being on a side of said reset transistor which is opposite to said first side. The difference between Kuriyama and the claimed invention is a halo implant below said single active area extension region and a threshold voltage adjustment implant in the channel region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (threshold voltage implant) 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of

Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous. It is also known that a halo (pocket) implant region affects the threshold voltage of a transistor. Therefore, it can be considered that the halo implant is also a threshold voltage adjustment implant. Note that it is considered that the "channel region" is the region between the source and drain.

Regarding claim 24, Figure 5 of Kuriyama discloses said photosensor 33 and said reset transistor are part of a transistor pixel circuit that further comprises a source follower transistor (amplification FET) and a row select transistor (select FET).

Regarding claim 26, Figure 5 of Kuriyama discloses a semiconductor substrate 30; a reset transistor (col. 11, lines 19-21) over said substrate; a floating diffusion region 34a in said substrate and in electrical communication with said reset transistor at a first side of said reset transistor; and a single active area extension region 34b in said substrate adjacent to said reset transistor, said single active area extension region being on a second side of said reset transistor which is opposite to said first side. The difference between Kuriyama and the claimed invention is a halo implant region in said substrate below said single active area extension region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed in the channel region (in the substrate 1) and below an LDD region. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous.

Regarding claims 27 and 43, the disclosure of Kuriyama does not explicitly disclose the image sensor is a CMOS imager. However, it would have been obvious to the ordinary artisan at the time the invention was made to use a CMOS imager as disclosed in the background of Kuriyama (col. 1, lines 18-25) for the purpose of integrating input elements with peripheral circuits on one chip.

Regarding claim 28, Figure 5 of Kuriyama discloses a photodiode 33 (col. 11, lines 64-66) in electrical contact with said reset transistor, said photodiode being within said substrate on said first side of said reset transistor.

Regarding claims 29 and 31, Kuriyama discloses an imaging device with an array of pixels (col. 2, lines 24-26). It can be considered that "a sensor array" includes all elements of each pixel (e.g., photosensors, transistors, diffusion regions). Therefore, the floating diffusion region is located within the sensor array. Alternatively, it can be considered that "a sensor array" only includes the photosensor portions of each pixel. In this case, the floating diffusion region is located outside the sensor array.

Regarding claims 38 and 39, Figure 1 of Kuriyama discloses a transistor (charge transfer transistor) (col. 5, lines 20-24) in contact with a photodiode 13 (col. 5, line 66 – col. 6, line 5) comprising a single active area extension 14b on a side of said transistor opposite from said photodiode. The difference between Kuriyama and the claimed invention is a halo implant below said single active area extension region and a threshold voltage adjustment implant below a gate of the transistor. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (threshold voltage implant) 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made

to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous. Furthermore, it is known that a halo (pocket) implant region affects the threshold voltage of a transistor. Therefore, it can be considered that the halo implant is also a threshold voltage adjustment implant.

Regarding claim 41, Figure 1 of Kuriyama discloses a source/drain region 14a and said active area extension region 14b are spaced away from a gate 12 of said first transistor by a portion 11 of a substrate 10/11 supporting said first transistor. Note that insulating film 11 can be considered to be part of the substrate.

Regarding claim 42, Figure 1 of Kuriyama discloses an insulating layer 15a/b over said transistor and said photodiode, said insulating layer extending to a floating diffusion region 14a adjacent to said active area extension region.

Regarding claim 45, Figure 1 of Kuriyama discloses said transistor (charge transfer transistor) (col. 5, lines 20-24) is part of a pixel having at least two other transistors (reset and select transistors) in electrical communication with said photodiode 13.

Regarding claims 50 and 51, Figure 1 of Kuriyama discloses a transistor (charge transfer transistor) (col. 5, lines 20-24) in electrical contact with a photodiode 13 (col. 5, line 66 – col. 6, line 5), said transistor comprising a single active area extension region 14b on a opposite side of said transistor from said photodiode and a source/drain region adjacent to said active area extension region, said active area extension region and said source/drain region being spaced away from a gate 12 of said transistor. Note that region 14b is spaced from the gate by the

insulating film 11. The difference between Kuriyama and the claimed invention is a halo implant below said single active area extension region and a threshold voltage adjustment implant below a gate of the transistor. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (threshold voltage implant) 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous. Furthermore, it is known that a halo (pocket) implant region affects the threshold voltage of a transistor. Therefore, it can be considered that the halo implant is also a threshold voltage adjustment implant.

Regarding claims 85 and 88, Figure 1 of Kuriyama discloses a transistor (charge transfer transistor) (col. 5, lines 20-24) comprising a channel region between a higher voltage side (right side) and a lower voltage side (left side), and a single active area extension region 14b at said higher voltage side of said channel. Note that it is inherent that the side (left side) with the photoconversion element 13 has a lower voltage than the side (right side) connected to the power source. The difference between Kuriyama and the claimed invention is a halo implant below said single active area extension region and a threshold voltage adjustment implant below a gate of the transistor. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (threshold voltage implant) 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made

to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous. Furthermore, it is known that a halo (pocket) implant region affects the threshold voltage of a transistor. Therefore, it can be considered that the halo implant is also a threshold voltage adjustment implant.

Regarding claim 86, Kuriyama discloses the transistor is part of a pixel (col. 5, lines 18-21).

Regarding claim 89, Figure 1 of Kuriyama discloses the transistor is associated with a photodiode 13 (col. 5, line 66 – col. 6, line 5) of a CMOS imager pixel.

Claims 15, 16, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama in view of Komuro and Park et al. (US Pat. 6,794,215, hereinafter Park).

Regarding claims 15 and 16, Figure 1 of Kuriyama discloses a semiconductor substrate 10; a transfer transistor (col. 5, lines 20-24) over said substrate, said transfer transistor having a single active area extension region 14b located on a first side (right side) of said transfer transistor; a photosensor 13 in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side; a reset transistor gate; and a floating diffusion region 14a on the first side of said transfer transistor and adjacent said reset transistor gate, said floating diffusion region in electrical communication with said active area extension region. Kuriyama does not

explicitly disclose that the reset transistor gate is over said substrate and spaced apart from said transfer transistor. Figure 1 of Park discloses a CMOS image sensor with both a transfer transistor Tx and a reset transistor Rx spaced apart from each other and on a substrate 11. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including the reset transistor on the substrate for the purpose of increasing the integration density. A further difference between Kuriyama and the claimed invention is a halo implant associated with the floating diffusion region and a threshold voltage adjustment implant in the channel region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (threshold voltage implant) 14 formed adjacent a source/drain region in the channel region. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous. It is also known that a halo (pocket) implant region affects the threshold voltage of a transistor. Therefore, it can be considered that the halo implant is also a threshold voltage adjustment implant. Note that it is considered that the "channel region" is the region between the source and drain.

Regarding claims 18 and 19, a further difference between Kuriyama and the claimed invention is said reset transistor comprises two active area extension regions as lightly doped drains on opposite sides of said reset transistor. Figure 5C of Komuro discloses LDD regions 5 on opposite sides of a MOS transistor. In view of such teaching, it would have been obvious to

the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including LDD regions on opposite sides of the reset transistor for the purpose of suppressing short channel effects and hot carrier generation, which is well known in the art. Note that a device having active area extension regions on both sides still reads on the limitation "a single active area extension region on a side opposite said floating diffusion region", since there is a single extension region on the opposite side. In other words, the opposite side does not have more than one extension region.

Regarding claim 20, Figure 1 of Kuriyama discloses a row select transistor (select FET).

Claims 1, 5, 15, 17, 32, 34, 37, 38, 40, 46, 48-52, 85, and 87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens in view of Kuriyama and Komuro.

Regarding claims 1 and 38, Figures 2 and 3 of Stevens disclose a photoconversion device PD; and a first transistor TG having a gate 76 with a first side (left side) and a second side (right side) opposite the first side, said gate being associated with (in electrical contact with) said photoconversion device (photodiode) at a first side of said first transistor. A difference between Stevens and the claimed invention is a single active area extension region on the second side with a halo implant below said extension region. Figure 1 of Kuriyama discloses a single active area extension region 14b (LDD region) on one side of a transfer transistor and a photodiode 13 (col. 5, lines 65-67) on the opposite side. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens by including an active area extension region (LDD region) on the second side of the first transistor

for the purpose of suppressing deterioration of the element properties (col. 6, lines 16-18 of Kuriyama). Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed below an active area extension region (LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Stevens and Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous.

Regarding claims 5 and 40, Figure 2 of Stevens discloses said first transistor TG has a gate length which is increased relative to other transistors (RG and unlabeled transistor to the right of transistor 100). Note that the instant application defines the gate length as the distance labeled 44 in Figure 1(a) (see paragraph [0033]). It is clear that the corresponding feature in Figures 2 and 3 of Stevens is larger in the first transistor TG than in the other two transistors indicated above.

Regarding claim 15, Figures 2 and 3 of Stevens disclose a semiconductor substrate 73; a transfer transistor TG over said substrate; a photosensor PD in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side; a reset transistor gate RG over said substrate and spaced apart from said transfer transistor; and a floating diffusion region 80 on the first side of said transfer transistor and adjacent said reset transistor gate. A difference between Stevens and the claimed invention is said transfer transistor having a single active area extension region located on a first side of said transfer transistor. Figure 1 of Kuriyama discloses a single

active area extension region 14b (LDD region) on one side of a transfer transistor and a photodiode 13 (col. 5, lines 65-67) on the opposite side. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens by including an active area extension region (LDD region) on the second side of the first transistor for the purpose of suppressing deterioration of the element properties (col. 6, lines 16-18 of Kuriyama). A further difference between Stevens and the claimed invention is having halo implant region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed below an active area extension region (LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Stevens and Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous.

Regarding claims 17 and 87, Figure 2 of Stevens discloses said first transistor TG has a gate length which is increased relative to other transistors (RG and unlabeled transistor to the right of transistor 100). Note that the instant application defines the gate length as the distance labeled 44 in Figure 1(a) (see paragraph[0033]). It is clear that the corresponding feature in Figures 2 and 3 of Stevens is larger in the first transistor TG than in the other two transistors indicated above.

Regarding claims 32, 34, 37, 46, and 48, Figures 2 and 3 of Stevens disclose a pixel array, at least one pixel of said array comprising: a photoconversion device (photodiode) PD, and a first transistor gate 76 (transfer transistor) in electrical contact with said photoconversion

device at a first side of said transistor gate, and said gate has a gate length which is increased relative to other transistors (RG and unlabeled transistor to the right of transistor 100). Note that the instant application defines the gate length as the distance labeled 44 in Figure 1(a) (see paragraph [0033]). It is clear that the corresponding feature in Figures 2 and 3 of Stevens is larger in the first transistor TG than in the other two transistors indicated above. It is inherent that the pixel array of Kuriyama supplies signals to some type of image processor. A difference between Stevens and the claimed invention is said transistor gate having a single active area extension region (LDD region) on a second side of said transistor gate opposite said first side. Figure 1 of Kuriyama discloses a single active area extension region 14b (LDD region) on one side of a transfer transistor and a photodiode 13 (col. 5, lines 65-67) on the opposite side. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens by including an active area extension region (LDD region) on the second side of the first transistor for the purpose of suppressing deterioration of the element properties (col. 6, lines 16-18 of Kuriyama). A further difference between Stevens and the claimed invention is a halo implant below said LDD region and a threshold voltage adjustment implant in the channel region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (threshold voltage implant) 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens and Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and

"halo" are synonymous. It is also known that a halo (pocket) implant region affects the threshold voltage of a transistor. Therefore, it can be considered that the halo implant is also a threshold voltage adjustment implant. Note that it is considered that the "channel region" is the region between the source and drain.

Regarding claim 49, Figures 2 and 3 of Stevens disclose a source/drain region 80. Note that both the active area extension region and the source/drain region will be spaced away from the gate 76 by a portion 74 of a substrate 73/74 (Figure 3 of Stevens). Note that insulating film 74 can be considered to be part of the substrate.

Regarding claims 50 and 51, the rejections of claims 46, 48, and claim 49 similarly apply to claims 50 and 51.

Regarding claim 52, Figures 2 and 3 of Stevens disclose the transistor TG and photodiode are part of a pixel cell (col. 2, lines 8-10) and transistor has a gate length which is increased relative to other transistors (RG and unlabeled transistor to the right of transistor 100). Note that the instant application defines the gate length as the distance labeled 44 in Figure 1(a) (see paragraph [0033]). It is clear that the corresponding feature in Figures 2 and 3 of Stevens is larger in the first transistor TG than in the other two transistors indicated above.

Regarding claim 85, Figures 2 and 3 of Stevens disclose a transistor TG comprising a channel region between a higher voltage side and a lower voltage side. Note that it is inherent that the side (left side) with the photoconversion element PD has a lower voltage than the side (right side) connected to the power source. A difference between Stevens and the claimed invention is said transfer transistor having a single active area extension region located on the higher voltage side of said transistor. Figure 1 of Kuriyama discloses a single active area

extension region 14b (LDD region) on one side of a transfer transistor and a photodiode 13 (col. 5, lines 65-67) on the opposite side. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens by including an active area extension region (LDD region) on the higher voltage side of the transistor for the purpose of suppressing deterioration of the element properties (col. 6, lines 16-18 of Kuriyama). A further difference between Stevens and the claimed invention is having halo implant region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed below an active area extension region (LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Stevens and Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous.

Response to Arguments

Applicant's arguments filed June 20, 2005 have been fully considered but they are not persuasive.

Applicant argues that the threshold voltage implant and halo implant region are not the same feature. However, as stated in the above rejection, it is known that a halo implant region will affect the threshold voltage of the device (see US PGPub 2004/0061187, paragraph [0008]). Therefore, it can be considered that a halo implant region is a threshold voltage implant. There

is nothing in the claim language that states the threshold voltage implant and the halo implant must be two separate and distinct regions. Applicant further argues that Kuriyama is directed to an imaging device, Komuro is directed only to a semiconductor device having a transistor, and that "there is noting in either reference to suggest the desirability or utility of utilizing the structure disclosed in Komuro with a photosensor structure like that disclosed by Kuriyama et al.". This is not persuasive since both Kuriyama and Komuro disclose MOS transistors. The fact that the transistor of Kuriyama is used in an imaging device does not mean the references cannot be combined. There is no reason why the features taught by Komura (specifically the pocket implant) cannot be incorporated into the transistor of Kuriyama. The problems solved by the pocket implant of Komura are common to all short channel transistors, including those in imaging devices. The motivation to combine these references was provided in the above rejection. Applicant further argues that the pocket doped region of Komuro is not a halo implant because a halo implant is "typically formed by a multi-angled, or at least multi-regional, implant". As stated in the above rejection, it is known in the art that the terms pocket implant and halo implant can be used interchangeably. In support of this claim, Applicant is directed to US Patent 6,417,550 (col. 2, lines 17 and 18) and US PGPub 2005/0077573 (paragraph [0005]). Both of these references disclose that a pocket implant is a halo implant. Furthermore, Applicant appears to be arguing that Koruma's implant region is made by a process different from that of the claimed implant region. Since the claims in question are device claims, the process by which the implant region is made cannot be used to patentably distinguish. In light of the above evidence and arguments, there is no reason why the pocket implant region of Koruma cannot be

considered a halo implant region. Applicant presents similar arguments regarding claims 21, 26, 32, 38, 50, and 85.

Applicant's arguments with respect to the Stevens reference have been considered but are moot in view of the new ground(s) of rejection. However, Applicant's arguments regarding the halo implant, and the Examiner's rebuttal of those arguments as set forth above, will apply to the new rejections.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6,417,550 and US PGPub 2005/0077573 both of disclose that a pocket implant is a halo implant. US PGPub 2004/0061187 discloses that a halo implant adjusts the threshold voltage (paragraph [0008]).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Matthew C. Landau

August 24, 2005